Tackling limited Test-Access problems on PCBs.

Functional testing is the original method of testing electronics. In the early days of the electronic industry, many systems were simply assembled and the power was switched on. By checking the functionality of the system, the ‘test’ was performed.
The growing complexity of modern systems has made functional test preparation a lengthy job, while the fault coverage of such test programs may remain unknown. Moreover, diagnosing faults found in functional testing can be very difficult, often requiring the help of a highly skilled technician.
Another test method is structural testing. By providing direct electrical access to the components on a PCB via a ‘bed of nails’ it is possible to test for manufacturing faults. This technique was well suited for DIP packages and through hole PCB technology. But along with the high density PCB using packages such as QFP and BGA test-access has become severely limited.
Fortunately, the industry anticipated these problems, and the Boundary-scan method was developed and adopted as the IEEE Standard 1149.1 Test Access Port and Boundary-scan Architecture.
The basic idea is simple enough – embed test ‘cells’ into a chip that can drive or capture a logic signal at the device pins, and access these via a serial scan chain shift register. By adding a state machine known as the JTAG TAP (Test Access Port) controller the data shifting and pattern generation/detection systems can be synchronised to enable an effective test to be performed at PCB and even system level.
Boundary-scan testing is in principle a structural test method that verifies whether the correct components are mounted on the board and whether all interconnects are present as defined in the design.
For the designer the biggest benefit is that he/she can now fully concentrate on the design. In production Boundary-scan is a fast test method, that delivers accurate diagnostics down to the component pin level.

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